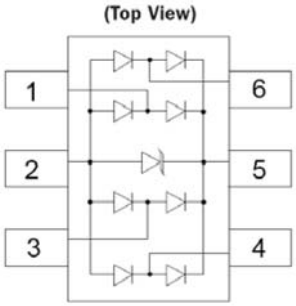
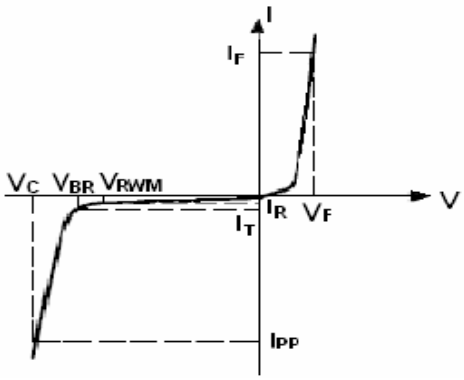
Description

- SES5VSC70-6U are surge rated diode arrays designed to protect high speed data interfaces. This device has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).
- The unique design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.
- The low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ± 8kV contact discharge).



Feature

- Array of surge rated diodes with internal TVS Diode
- SC-70-6 Package
- Protects up to four I/O lines & power line
- Low capacitance (<2pF) for high-speed interfaces
- No insertion loss to 2.0GHz
- Low leakage current and clamping voltage
- Low operating voltage: 5.0V
- Solid-state silicon-avalanche technology
- Transient protection for data lines to IEC 61000-4-2(ESD) ±15KV(air), ±8KV(contact); IEC 61000-4-4 (EFT) 40A (5/50ns)



Applications

- USB 2.0
- USB OTG
- Monitors and Flat Panel Displays
- Displays Digital Visual Interface (DVI)
- High-Definition Multimedia Interface (HDMI)
- Gigabit Ethernet
- SIM Ports
- IEEE 1394 Firewire Ports

Electrical characteristics per line@25℃(unless otherwise specified) note1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse stand-off voltage	V_{RWM}	Pin 5 to 2			5	V
Reverse Breakdown voltage	V_{BR}	I_t = 1mA Pin 5 to 2	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V T=25℃ Pin 5 to 2			2	μA
Clamping Voltage	V_C	I_{PP} = 1A t_P = 8/20μs Any pin to 2			15	V
Clamping Voltage	V_C	I_{PP} = 6A t_P = 8/20μs Any pin to 2			25	V
Junction Capacitance	C_j	V_R=0V f = 1MHz Any I/O pin to pin 2		2		pF
		V_R=0V f = 1MHz Between I/O pins		1		pF

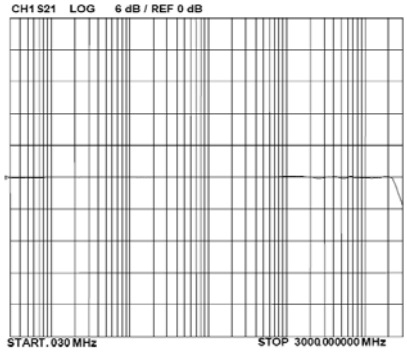
- Note 1: I/O pins are pin 1, 3, 4, and 6

Absolute maximum rating @25℃

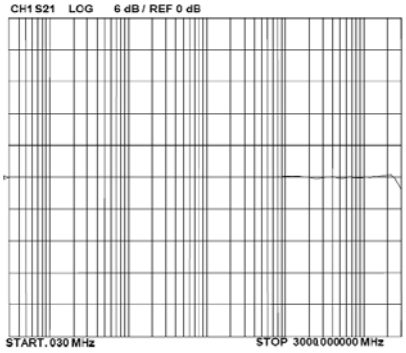
Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μs)	P_{pp}	150	W
Peak Pulse Current (t_p=8/20μs)	I_{PP}	6	A
Operating Temperature	T_J	-55 to +150	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Typical Characteristics

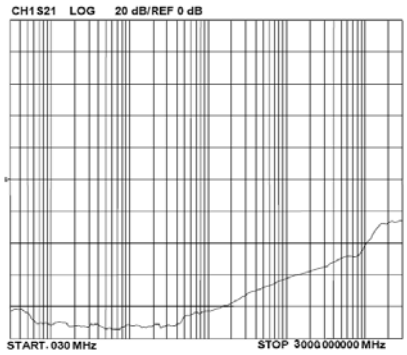
Insertion Loss S21 (I/O to Pin 2)



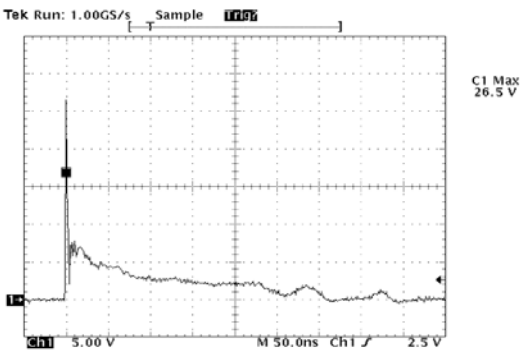
Insertion Loss S21 (I/O to I/O)



Analog Crosstalk

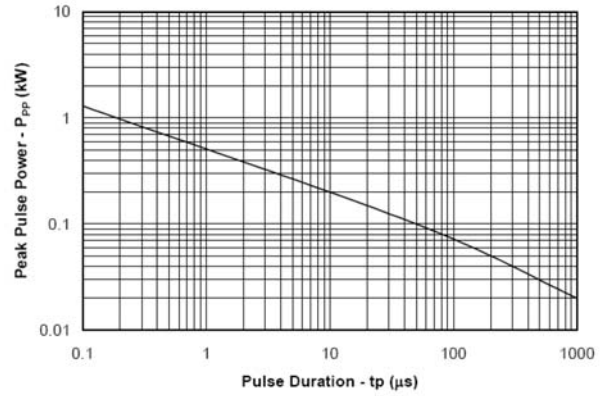


ESD Response (8kV Contact per IEC 61000-4-2)

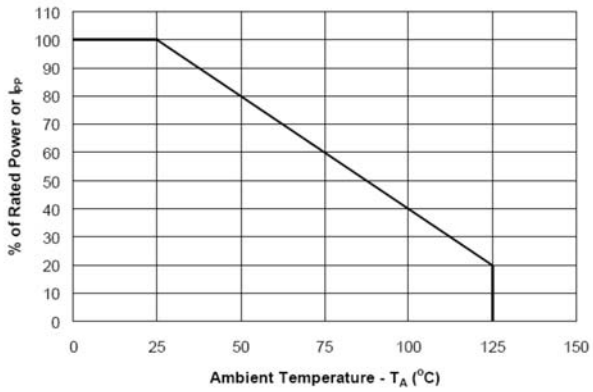


Typical Characteristics

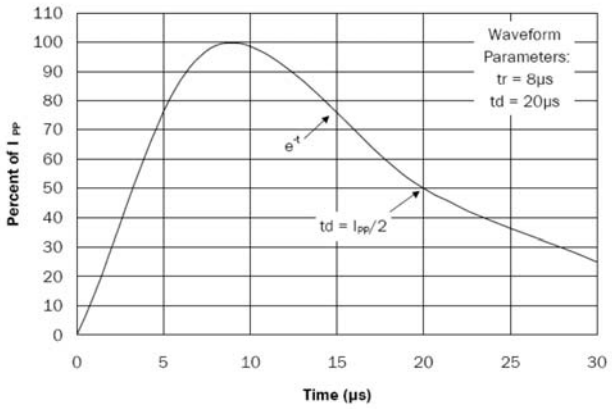
Non-Repetitive Peak Pulse Power vs. Pulse Time



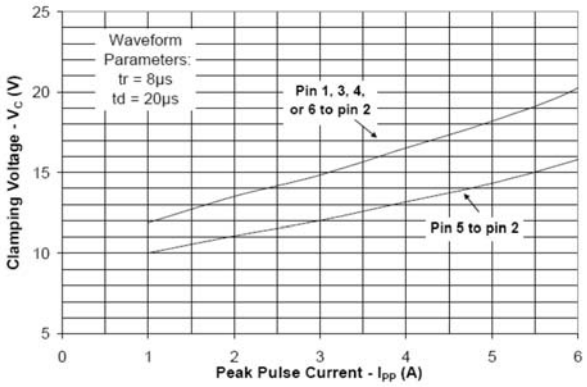
Power Derating Curve



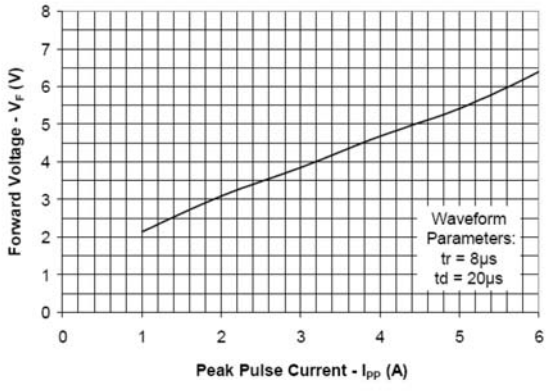
Pulse Waveform



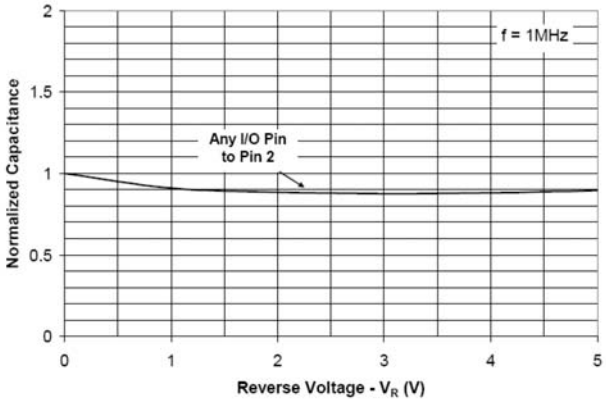
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. peak Pulse Current



Capacitance vs. Reverse Voltage (Normalized to 0V)



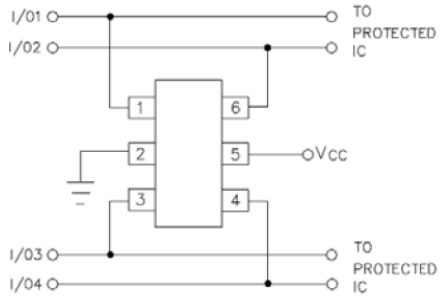
Application Information

Device Connection Options for Protection of Four High-Speed Data Lines

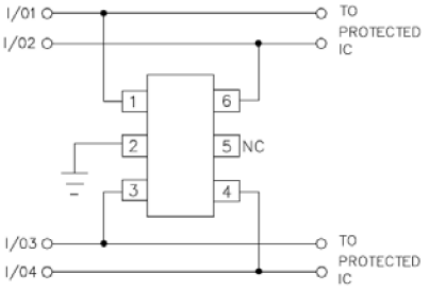
This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. Pin 2 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).
3. In applications where complete supply isolation is desired, the internal TVS is again used as the reference and V_{CC} is connected to one of the I/O inputs. An example of this configuration is the protection of a SIM port. The Clock, Reset, I/O, and VCC lines are connected at pins 1, 3, 4, and 6. Pin 2 is connected to ground and pin 5 is not connected.

Protection of Four Data Lines and Power Supply Line



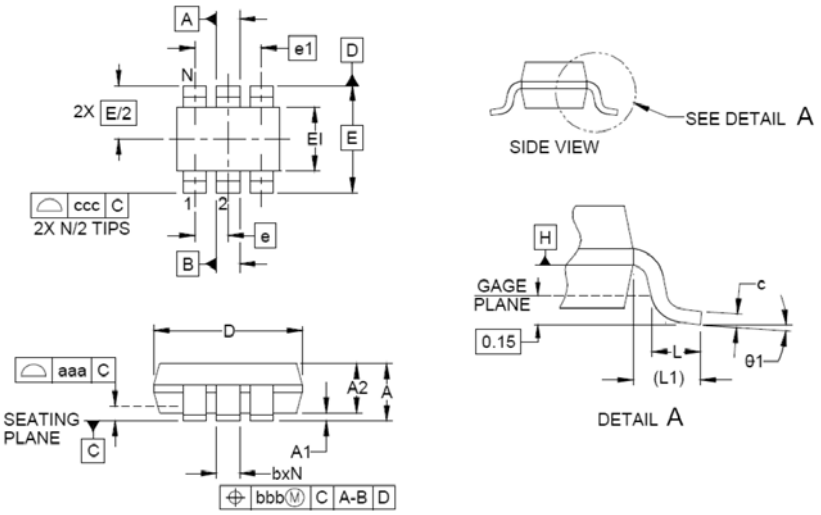
Protection of Four Data Lines Using Internal TVS Diode as Reference



Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

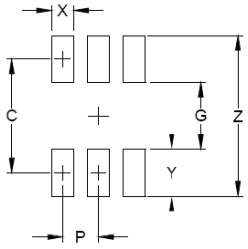
Product dimension and pad size



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.004	0.00	-	0.10
A2	.028	.035	.039	0.70	0.90	1.00
b	.006	-	.012	0.15	-	0.30
c	.003	-	.009	0.08	-	0.22
D	.075	.079	.083	1.90	2.00	2.10
E1	.045	.049	.053	1.15	1.25	1.35
E	.083 BSC			2.10 BSC		
e	.026 BSC			0.65 BSC		
e1	.051			1.30 BSC		
L	.010	.014	.018	0.26	0.36	0.46
L1	(.017)			(0.42)		
N	6			6		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.012			0.30		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-203, VARIATION AB.



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.073)	(1.85)
G	.039	1.00
P	.026	0.65
X	.016	0.40
Y	.033	0.85
Z	.106	2.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Revision History

Revision	Date	Changes
1.0	2008-7-3	-