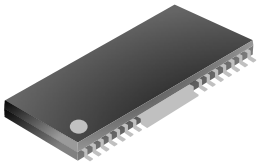
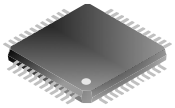
2×10W CLASS-D AUDIO POWER AMPLIFIER

DESCRIPTION

SD7408 is a 2×10W analog input Class-D audio power amplifier for driving bridged-tied stereo speakers.
Thanks to the high efficiency and HSOP-28 / ELQFP-48 Packages, no heatsink is require.
Furthermore, the filterless operation allows a reduction in the external component count.



HSOP - 28-375-0.8



ELQFP-48-7×7-0.5
(With heatsink at the bottom)

FEATURES

* Output Power:
  2×9.5W @ V_{CC}=12V, R_L=8Ω, THD=10%;
  2×10.5W @ V_{CC}=17V, R_L=16Ω, THD=10%
* Supply Voltage: 8.5V to 18V
* Efficiency: Up to 90%
* Four Selectable,Fixed Gain Settings of 15.3, 21.2, 27.2, 31.8dB
* Differential Inputs
* Filterless Operation
* Shutdown Function
* Fully Protected against shorts to VCC, GND and OUT-to-OUT
* Thermal Protection

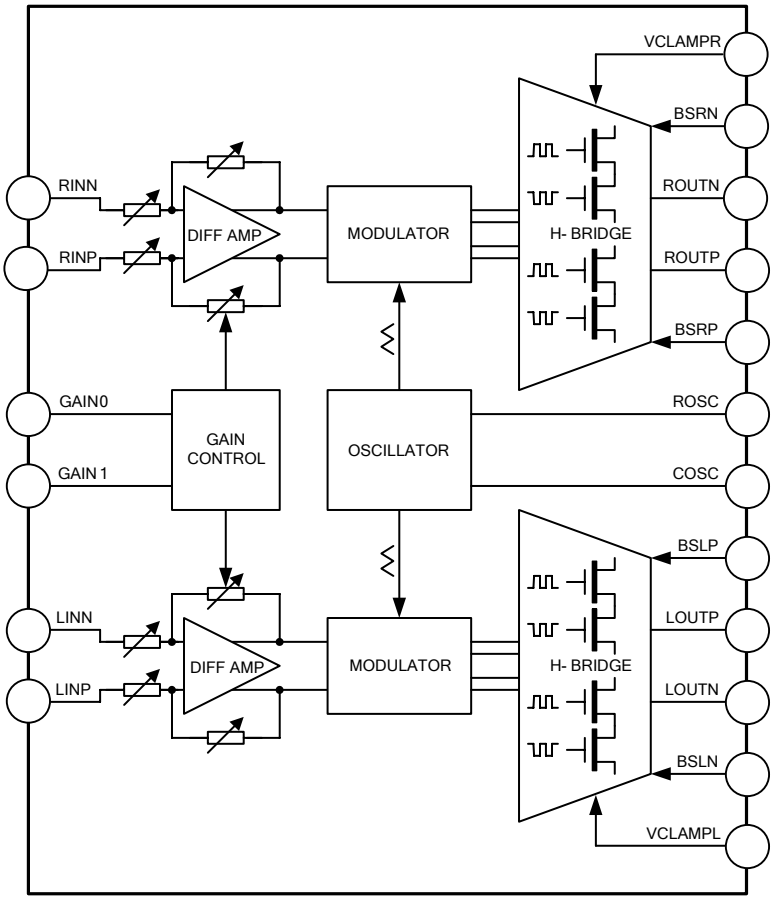
APPLICATIONS

* Multimedia System
* LCD Monitor and TV

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SD7408	HSOP-28-375-0.8	SD7408	Pb free	Tube
SD7408TR	HSOP-28-375-0.8	SD7408	Pb free	Tape & Reel
SD7408LS	ELQFP-48-7×7-0.5	SD7408LS	Pb free	Tray
SD7408LSTR	ELQFP-48-7×7-0.5	SD7408LS	Pb free	Tape & Reel

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

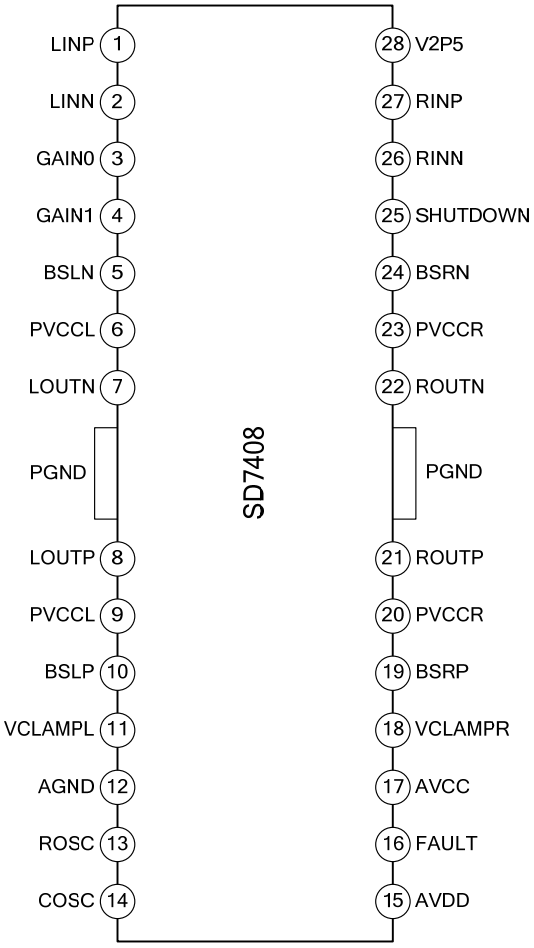
Characteristics	Symbol	Rating		Unit
Power Supply	AV_{CC} PV_{CC}	20		V
Load Impedance	R_L	≥ 6		Ω
Total Power Dissipation	Pdiss	2.5		W
Storage Temperature	T_{stg}	-55~+150		°C
Operating Ambient Temperature	T_{amb}	-40~+85		°C
Junction Temperature	T_j	+150		°C
Thermal Resistance from Junction to Ambient	$R_{th(j-a)}$	SD7408	30	°C/W
		SD7408LS	50	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC}=12V; R_L=8Ω; f=1KHz; T_{amb}=25°C)

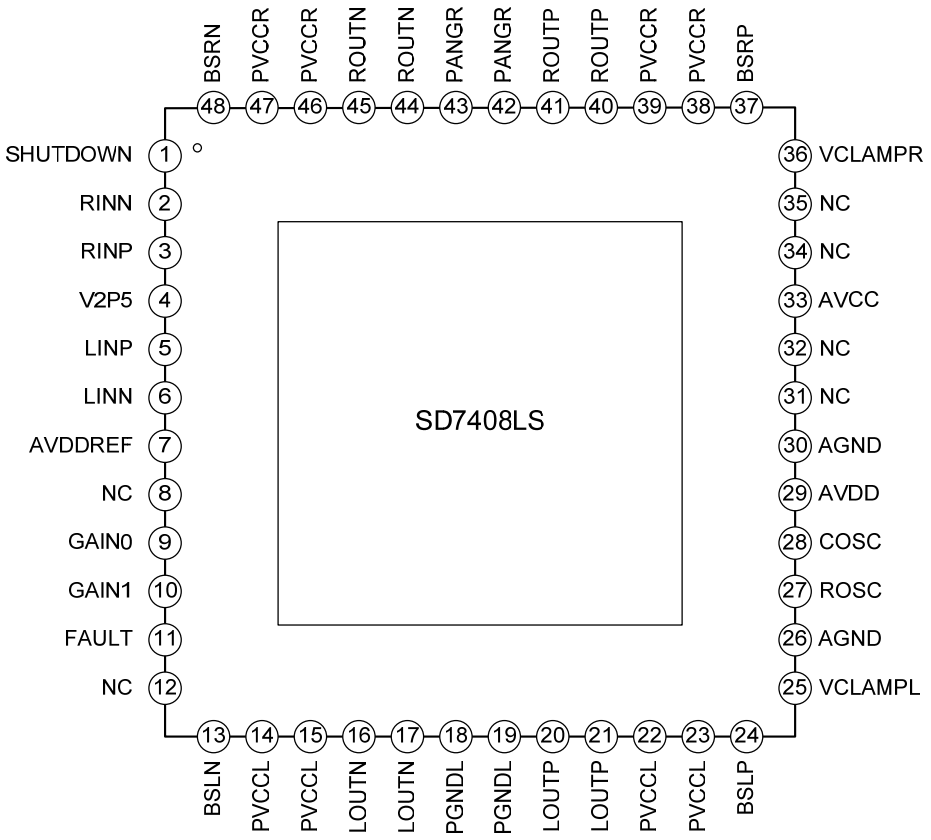
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply Voltage	AV_{CC} PV_{CC}		8.5	12.0	18.0	V
Quiescent Supply Current	I_Q	SD=2V, filterless operation and no load		10	15	mA
Quiescent Supply Current In Shutdown Mode	$I_{Q(SD)}$	SD=0V		1.0	25	μA
5V Internal Supply Voltage	AV_{DD}	I_L=10mA, SD=2V, V_{CC}=8.5V~18V	4.5	5.0	5.5	V
2.5V Bias Voltage	V2P5	No load		2.5		V
Drain-Source On-State Resistance	$R_{DS(on)}$	I_O=1A, High side		300		mΩ
		I_O=1A, Low side		300		
		Total		600	800	
Switching Frequency	fsw	Set by ROSC and COSC	200		300	kHz
Output Power	P_O	THD=1%, RL=8Ω		7.5		W
		THD=10%, RL=8Ω		9.5		
		THD=1%, RL=16Ω, V_{CC}=17V		8.5		
		THD=10%, RL=16Ω, V_{CC}=17V		10.5		
Total Harmonic Distortion	THD	P_O=1W, RL=8Ω		0.1	0.3	%
		P_O=1W, RL=16Ω, V_{CC}=17V		0.1	0.3	
Efficiency	η	P_O=9.5W, RL=8Ω		90		%
		P_O=10W, RL=16Ω, V_{CC}=17V		94		
Power Supply Rejection Ratio	PSRR	200mV_{PP} ripple from 20Hz to 1kHz, G_V =15.6dB, Inputs ac-coupled to GND		-65		dB
Output Noise	V_{no}	20Hz to 22kHz, A-weighted filter, G_V =15.6dB		-75		dBVrms
Channel Separation	CS	P_O=1W, G_V=15.6dB		-70		dB
Channel Balance	CB	P_O=1W, G_V=15.6dB		0.1	1	dB
Thermal Point				150		°C
Thermal Hystersis				20		°C
Shutdown Function (SHUTDOWN)						
High-Level Input Voltage	V_{IH}		2			V
Low-Level Input Voltage	V_{IL}				0.8	V
High-Level Input Current	I_{IH}	V_I=V_{CC}=18V			10	μA
Low-Level Input Current	I_{IL}	V_I=0V, V_{CC}=18V			1	μA
Turn On Time	t_{on}	$C_{(V2P5)}$=0.47μF, SD=2V		16		ms
Turn Off Time	t_{off}	$C_{(V2P5)}$=0.47μF, SD=0.8V		60		μs

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Gain settings Function (GAIN0, GAIN1)						
High-Level Input Voltage	V_{IH}		2			V
Low-Level Input Voltage	V_{IL}				0.8	V
High-Level Input Current	I_{IH}	V_I=5.5V, V_{CC}=18V			1	μA
Low-Level Input Current	I_{IL}	V_I=0V, V_{CC}=18V			1	μA
Gain	G_V	GAIN1=0.8V, GAIN0=0.8V	14.6	15.3	16.2	dB
		GAIN1=0.8V, GAIN0=2V	20.5	21.2	21.8	
		GAIN1=2V, GAIN0=0.8V	26.4	27.2	27.8	
		GAIN1=2V, GAIN0=2V	31.1	31.8	32.5	
Short-circuit Protected **Function (FAULT)**						
High-Level Output Voltage	V_{OH}	I_{OH}=100μA	AVDD-0.8V			V
Low-Level Output Voltage	V_{OL}	I_{OL}=-100μA			AGND+0.8V	V

PIN CONFIGURATION



PIN CONFIGURATION (continued)



PIN DESCRIPTIONS

Pin No.		Pin Name	I/O	Pin Description
SD7408	SD7408LS			
25	1	SHUTDOWN	I	Shutdown control TTL logic levels with compliance to AVCC
26	2	RINN	I	Negative input for right channel
27	3	RINP	I	Positive input for right channel
28	4	V2P5	O	2.5V reference
1	5	LINP	I	Positive input for left channel
2	6	LINN	I	Negative input for left channel
--	7	AVDDREF	O	5V Reference output
--	8	NC	--	No internal connection
3	9	GAIN0	I	Gain select least significant bit. TTL logic levels with compliance to AVDD
4	10	GAIN1	I	Gain select most significant bit. TTL logic levels with compliance to AVDD
16	11	FAULT	O	Short-circuit detect fault output

Pin No.		Pin Name	I/O	Pin Description
SD7408	SD7408LS			
--	12	NC	--	No internal connection
5	13	BSLN	--	Bootstrap I/O for left channel, negative high-side FET
6	14	PVCCL	--	Power supply for left channel H-bridge
	15			
7	16	LOUTN	O	Class-D 1/2-H-bridge negative output for left channel
	17			
--	18	PGNDL	--	Power ground for left channel H-bridge
	19			
8	20	LOUTP	O	Class-D 1/2-H-bridge positive output for left channel
	21			
9	22	PVCCL	--	Power supply for left channel H-bridge
	23			
10	24	BSLP	--	Bootstrap I/O for left channel, positive high-side FET
11	25	VCLAMPL	--	Internally generated voltage supply for left channel bootstrap capacitors
12	26	AGND	--	Analog ground for analog/digital cells in core
13	27	ROSC	I/O	I/O current setting resistor for oscillator
14	28	COSC	I/O	I/O for charge/discharging currents onto capacitor for oscillator
15	29	AVDD	O	5V regulated output
--	30	AGND	--	Internally Test Signal setting to AGND
--	31	NC	--	No internal connection
--	32	NC	--	No internal connection
17	33	AVCC	--	High voltage analog power supply
--	34	NC	--	No internal connection
--	35	NC	--	No internal connection
18	36	VCLAMPR	--	Internally generated voltage supply for right channel bootstrap capacitors
19	37	BSRP	--	Bootstrap I/O for right channel, positive high-side FET
20	38	PVCCR	--	Power supply for right channel H-bridge
	39			
21	40	ROUTP	O	Class-D 1/2-H-bridge positive output for right channel
	41			
--	42	PGNDR	--	Power ground for right channel H-bridge
	43			
22	44	ROUTN	O	Class-D 1/2-H-bridge negative output for right channel
	45			
23	46	PVCCR	--	Power supply for right channel H-bridge
	47			

Pin No.		Pin Name	I/O	Pin Description
SD7408	SD7408LS			
24	48	BSRN	--	Bootstrap I/O for right channel, negative high-side FET
--	--	PGND	--	Power ground of HSOP-28 Package,connect to GND
--	--	Thermal Pad	--	Thermal Pad of ELQFP-48 Package,connect to GND

FUNCTION DESCRIPTION

Shutdown Operation

The SD7408 employs a shutdown mode of operation designed to reduce supply current (ICC) to the absolute minimum level during periods of nonuse for power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SHUTDOWN unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

Gain setting via GAIN0 and GAIN1 inputs

The gain of the SD7408 is set by two input terminals: GAIN0 and GAIN1.The gains listed in Table 1 are realized by changing the ratios of resistors inside the amplifier. This causes the input impedance (Zi) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation is small due to process shifts. Howerer, the actual input impedance may shift by ±20% comparing with typical value.

For meeting all the input impedance situations, the input network (discussed in the next section) should be designed assuming an input impedance of 26kΩ, which is the absolute minimum input impedance of the SD7408.

Table 1 Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB) (TYP)	INPUT IMPEDANCE (kΩ) (TYP)
0	0	15.3	137
0	1	21.2	88
1	0	27.2	52
1	1	31.8	33

Input Capacitor, Ci

In the typical application, an input capacitor (Ci) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, Ci and the input impedance (Zi) for a high-pass filter with the corner frequency determined in Equation:

$$f_C = \frac{1}{2\pi Z_i C_i}$$

The value of Ci is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Zi is 26kΩ and the specification calls for a flat bass response down to 20Hz. Solving Equation gives Ci = 0.3μF.

A further consideration for the capacitor is the leakage path from the input source through the input network (Ci)

and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice.
When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.5V, which is likely higher than the source dc level. Not that it is important to confirm the capacitor polarity in the application.
For the best pop performance, Ci should be less than or equal to 1μF.

Differential Input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the SD7408 with a differential source, connect the positive lead of the audio source to the INP and the negative lead from the audio source to the INN. To use the SD7408 with a single-ended source, ac ground the INP or INN through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance.

Power Supply Decoupling, Cs

SD7408 requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digita hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the decice VCC lead works best. For filtering lower frequency noise signals, a larger aluminum elecrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended. The 10μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input.
The bootstrap capacitors connected between the BS pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, two internal regulators clamp the gate voltage. Two 1μF capacitors must be connected from VCLAMPL and VCLAMPR to ground and must be rated for at least 25V.

Internal Regulated 5V Supply (AVDD)

The AVDD terminal is the output of an internally generated 5V supply, used for the oscillator, preamplifier, and volume control circuitry. It requires a 1μF capacitor, placed close to the pin, to keep the requlator stable.
This requlated voltage can be used to control GAINo and GAIN1 terminals, but should not be used to drive external circuitry.

Short-Cirvuit Protection and Automatic Recovery Feature

The SD7408 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-VCC shorts. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the SHUTDOWN pin to a logic low and back to the logic high state for normal operation, This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

FAULT pin of SD7408 can be used to monitor the status: FAULT = high, short-circuit detected; FAULT = low, normal operation. Also It can be used to control SHUTDOWN pin for automatic recovery from a short-circuit event.

Thermal Protection

Thermal protection on the SD7408 prevents damage to the device when the internal die temperature exceeds 150°C. Once the die tempetature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20 ℃. The device begins normal operation at this point with no external system interaction.

Use an Output Filter for EMI Suppression

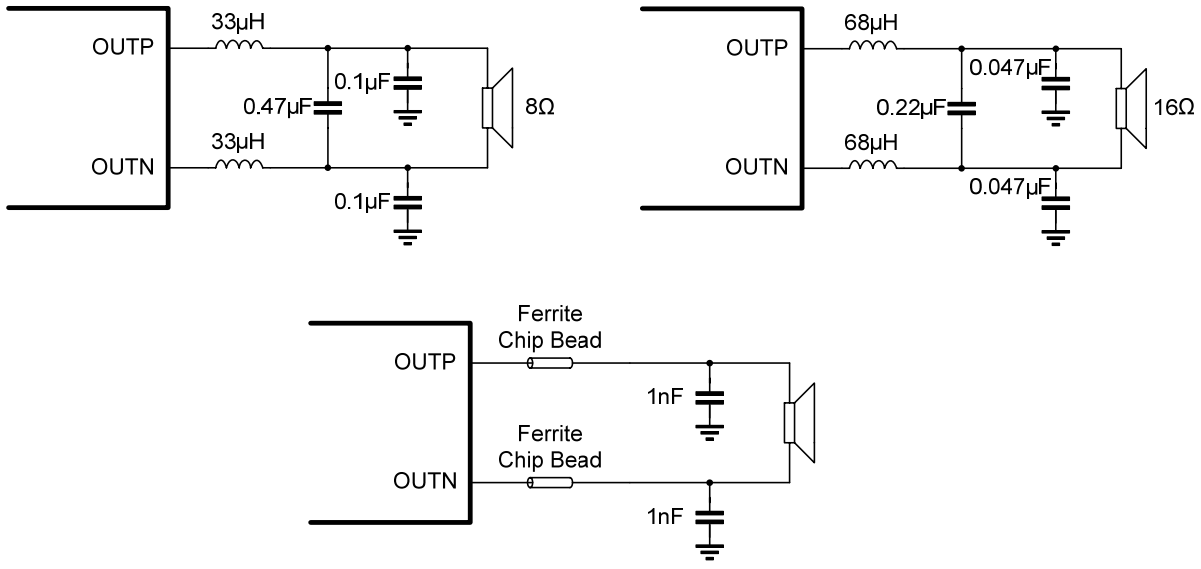
Design the SD7408 without the filter if the traces from amplifier to speaker are short (< 50cm). Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1MHz and higher (FCC and CE only test radiated emissions greater than 30MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

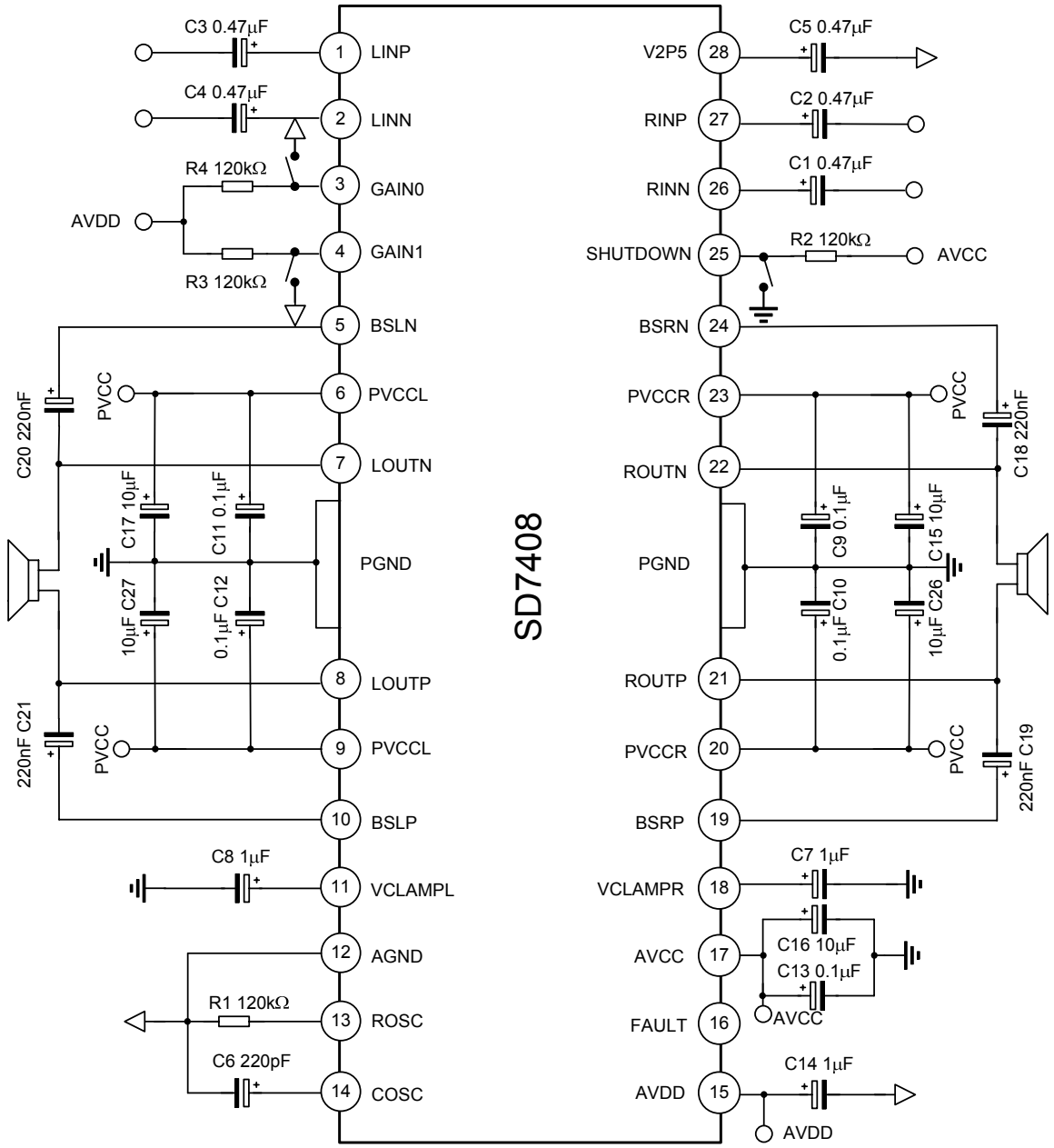
Use a LC output filter if there are low frequency (<1MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker.

When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

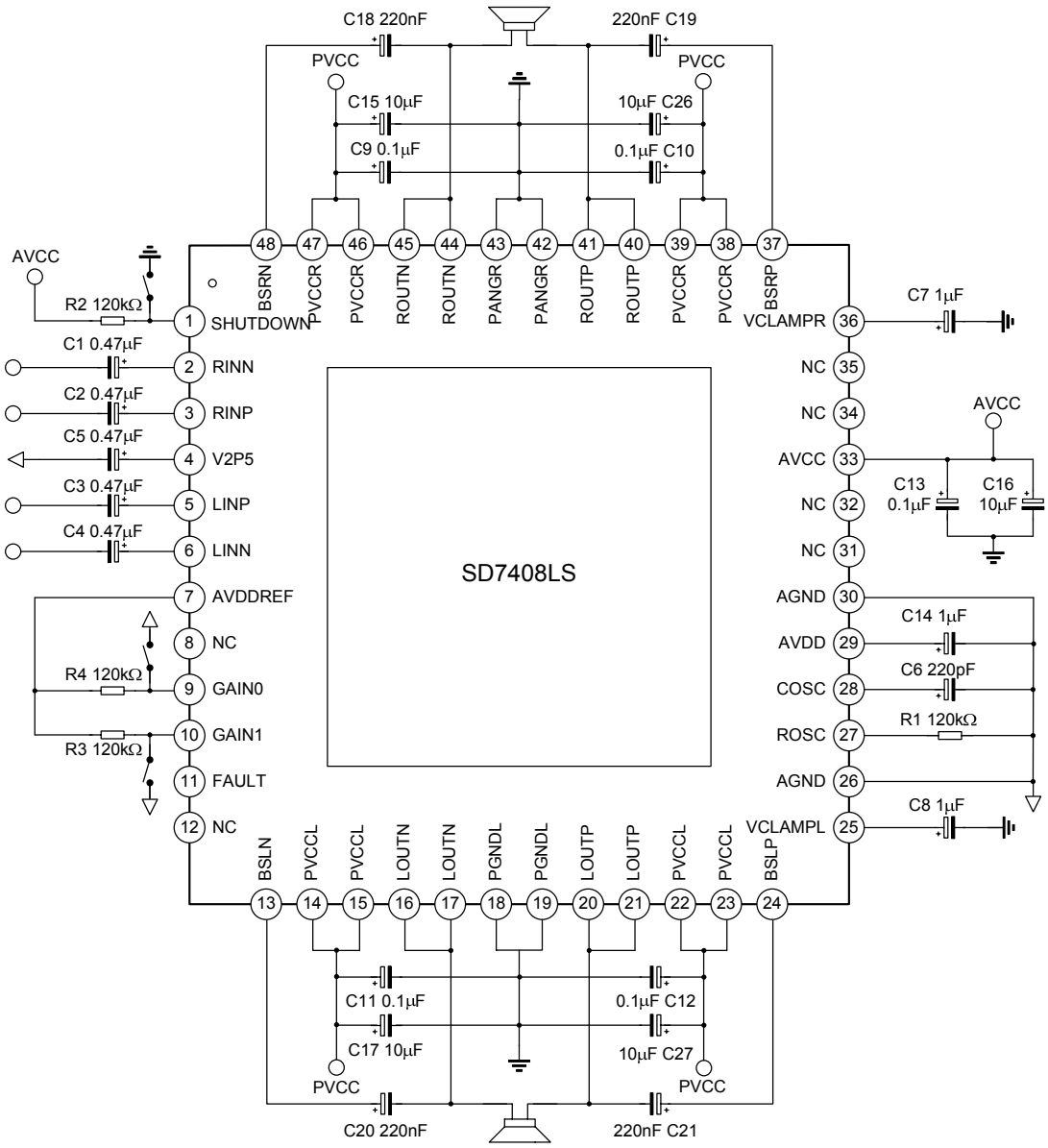
Settings of an LC filter for a 8Ω and 16Ω speaker and a ferrite bead filter as follows:



TYPICAL APPLICATION CIRCUIT

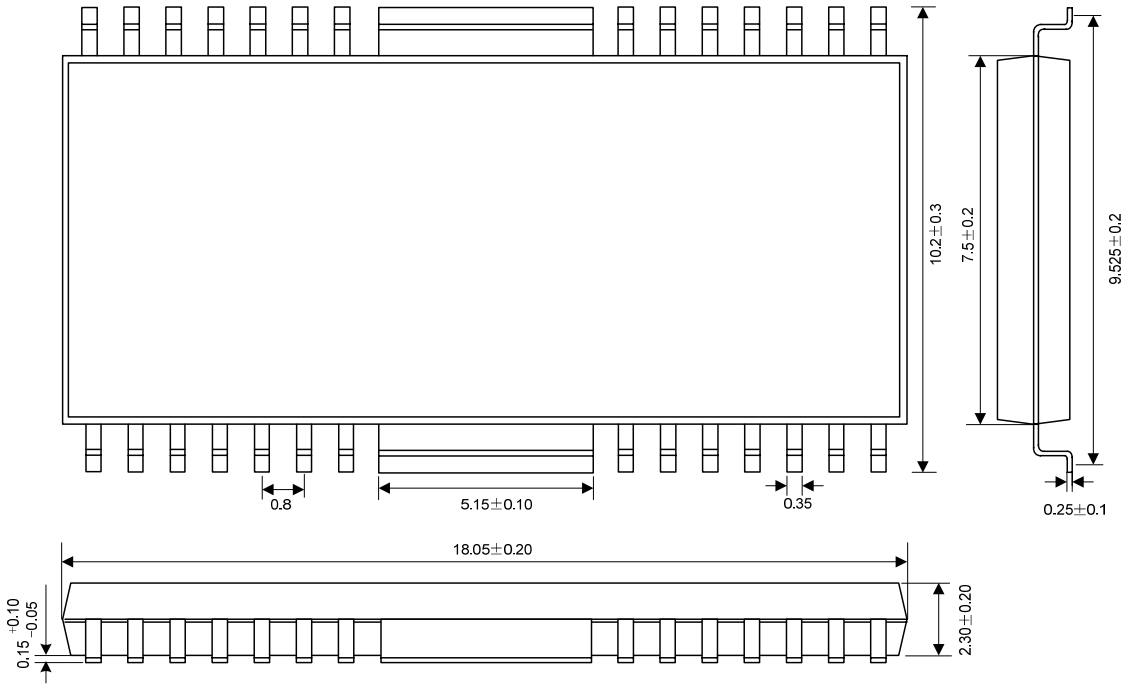


TYPICAL APPLICATION CIRCUIT (continued)

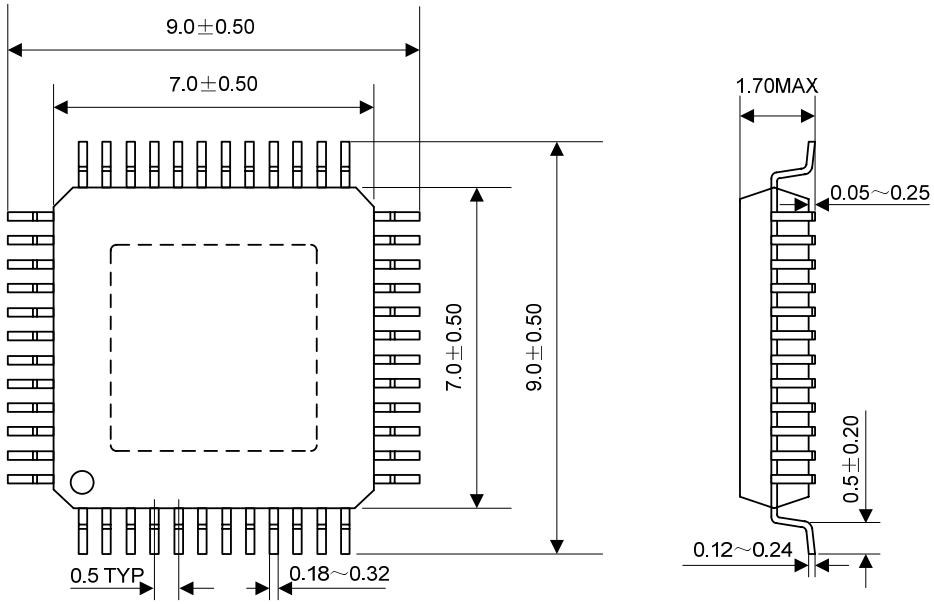


PACKAGE OUTLINE

HSOP-28-375-0.8 Unit: mm



ELQFP-48-7×7-0.5 Unit: mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.